



FIG. 1

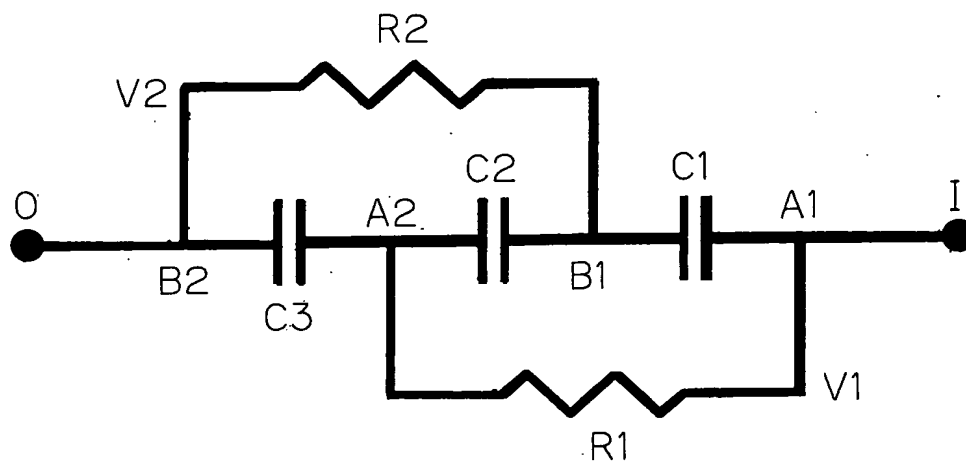


FIG. 2

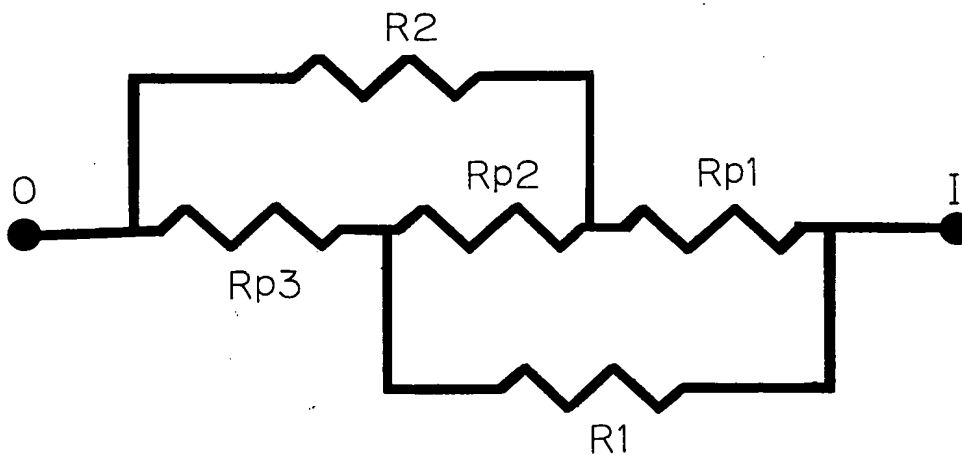


FIG. 3

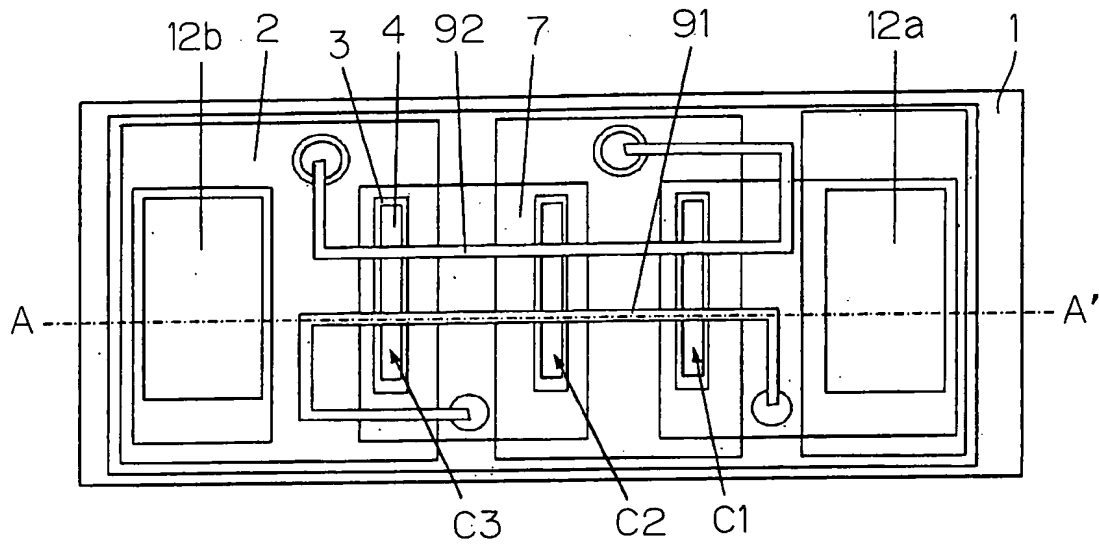


FIG. 4

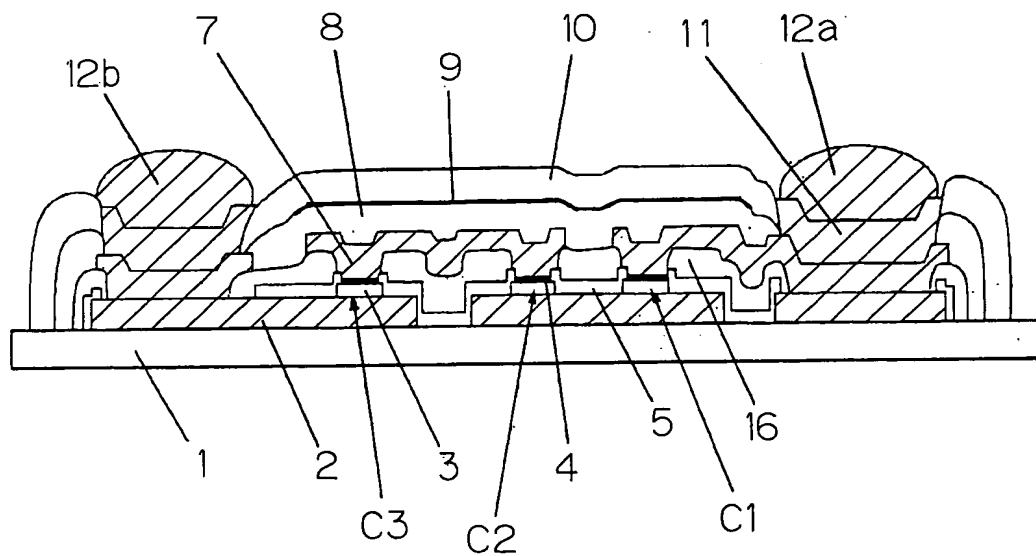


FIG. 5

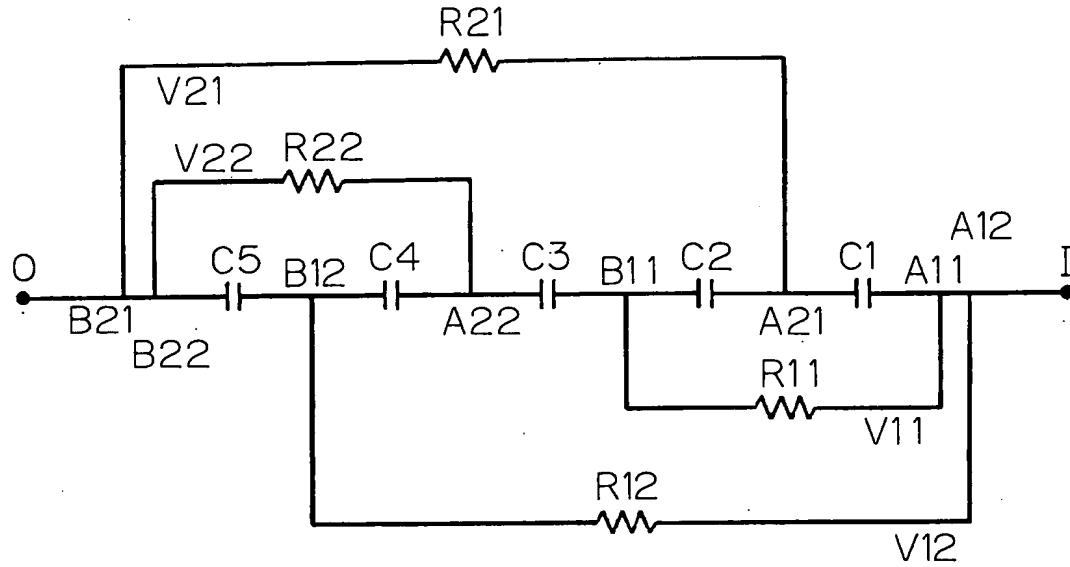


FIG. 6

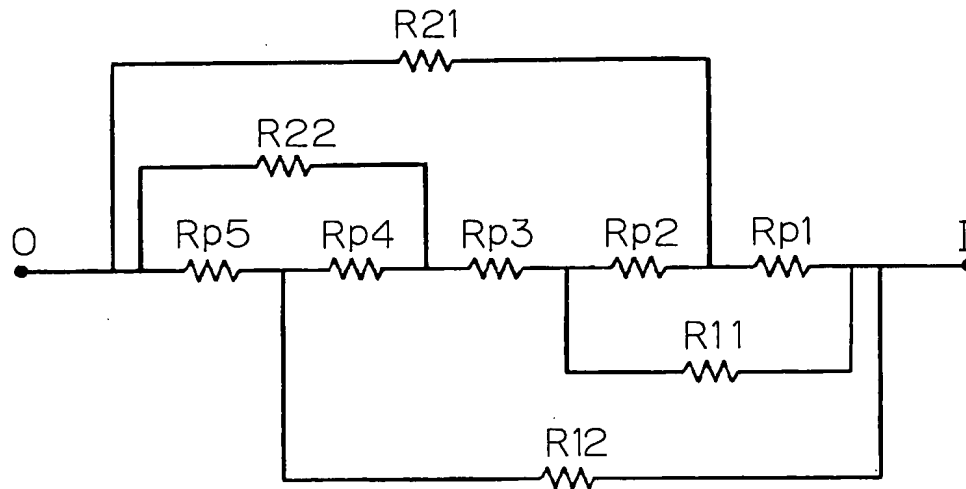


FIG. 7

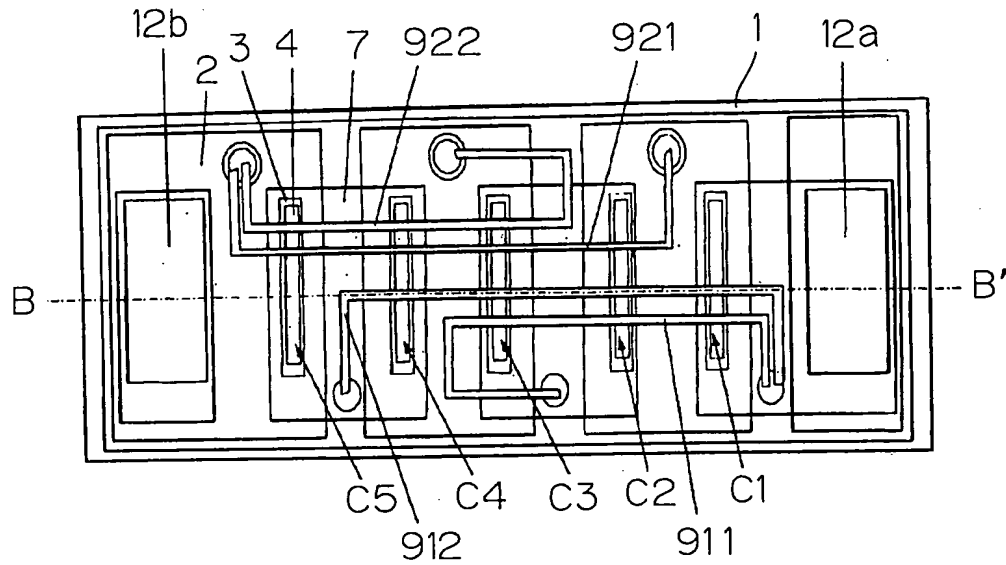


FIG. 8

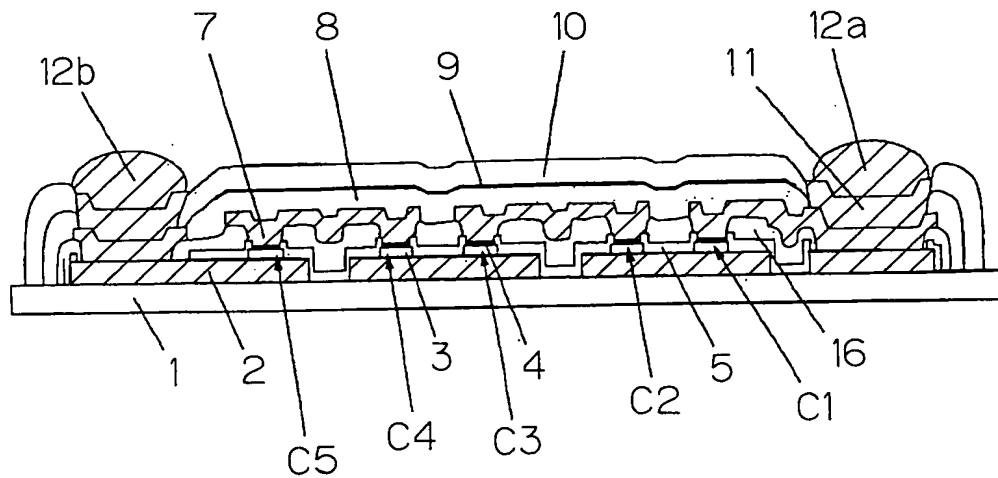


FIG. 9

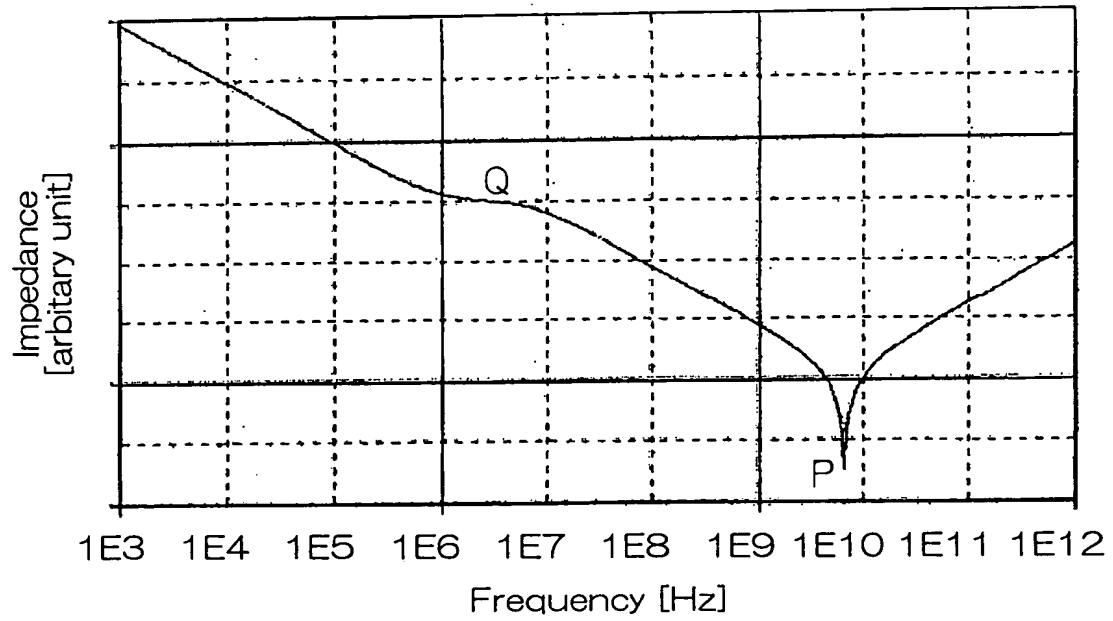
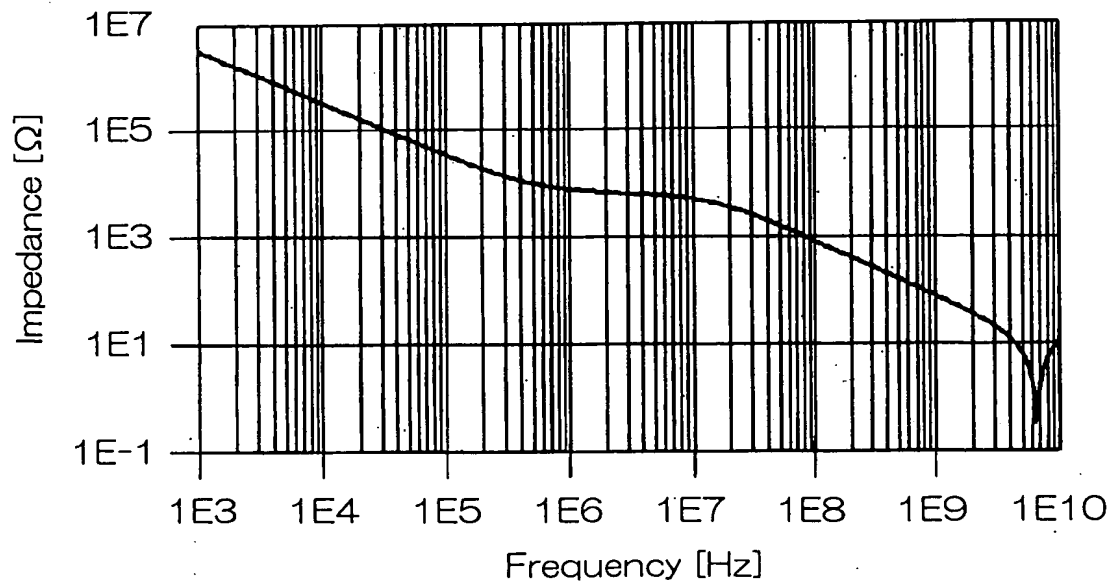


FIG. 10



This cross-sectional view shows a multi-layer printed circuit board assembly. A central conductive layer (1) is sandwiched between multiple dielectric layers (2). The assembly is protected by a top layer (3) and a bottom layer (4). A central conductive pad (5) is connected to the central conductive layer (1) via a through-hole (6). The top and bottom layers (3 and 4) are connected to the central conductive layer (1) via vias (7). The top and bottom layers (3 and 4) are also connected to the central conductive layer (1) via vias (8). The top and bottom layers (3 and 4) are also connected to the central conductive layer (1) via vias (9). The top and bottom layers (3 and 4) are also connected to the central conductive layer (1) via vias (10). The top and bottom layers (3 and 4) are also connected to the central conductive layer (1) via vias (11). The top and bottom layers (3 and 4) are also connected to the central conductive layer (1) via vias (12a and 12b).

FIG. 13

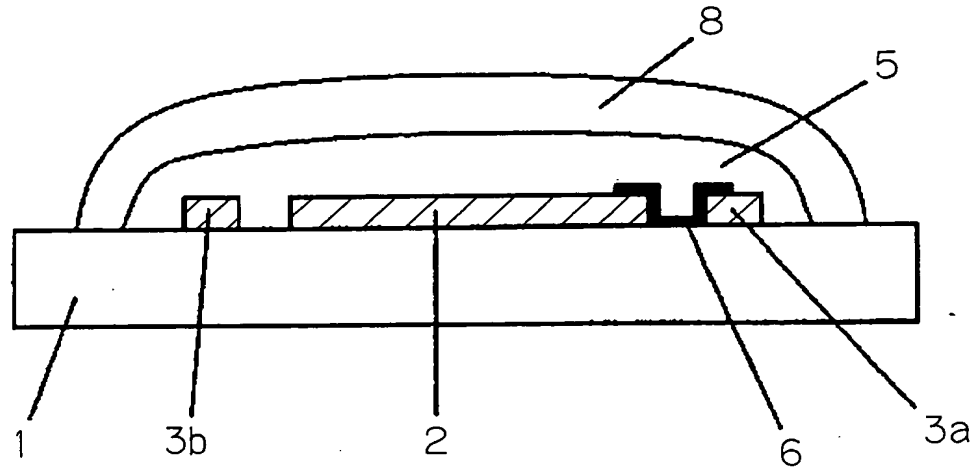


FIG. 14

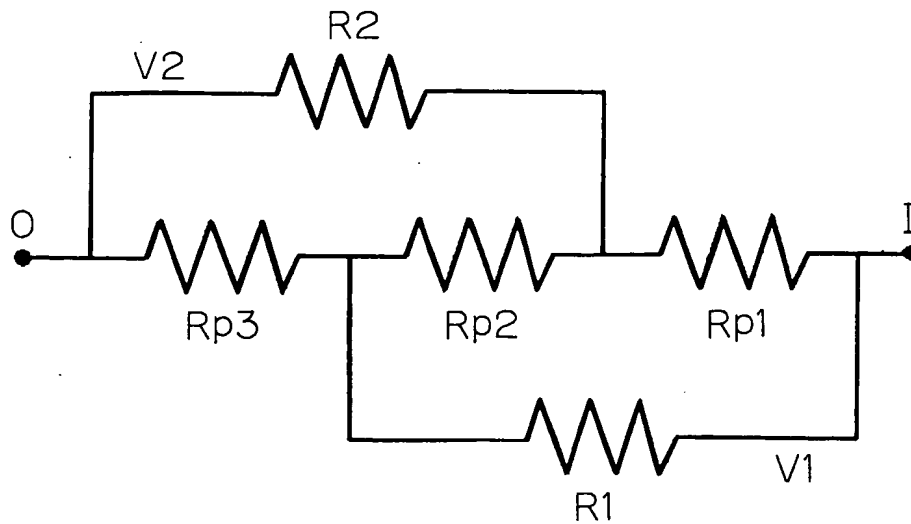


FIG. 15

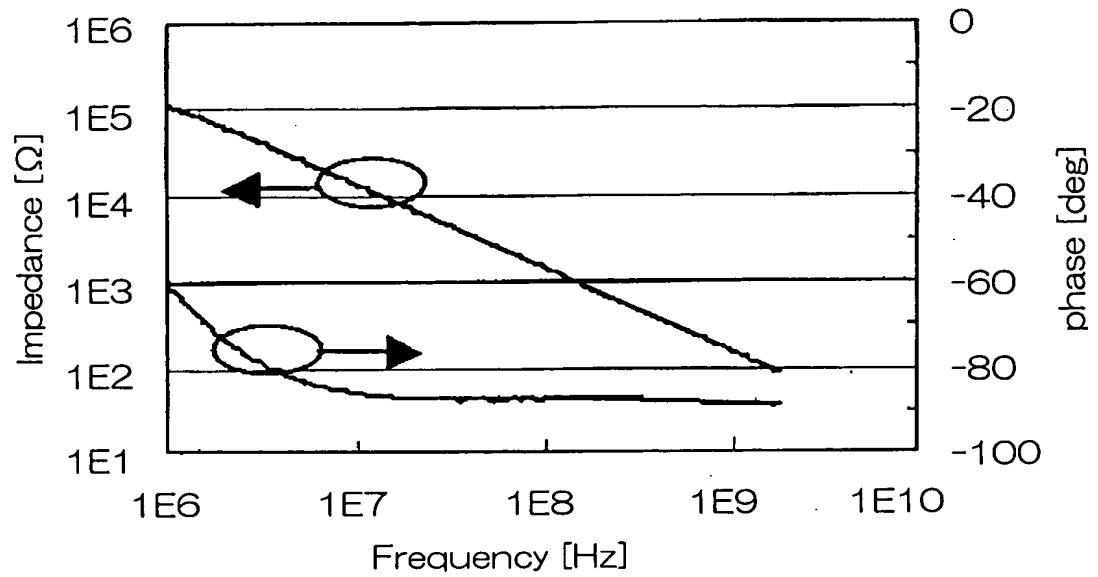


FIG. 16

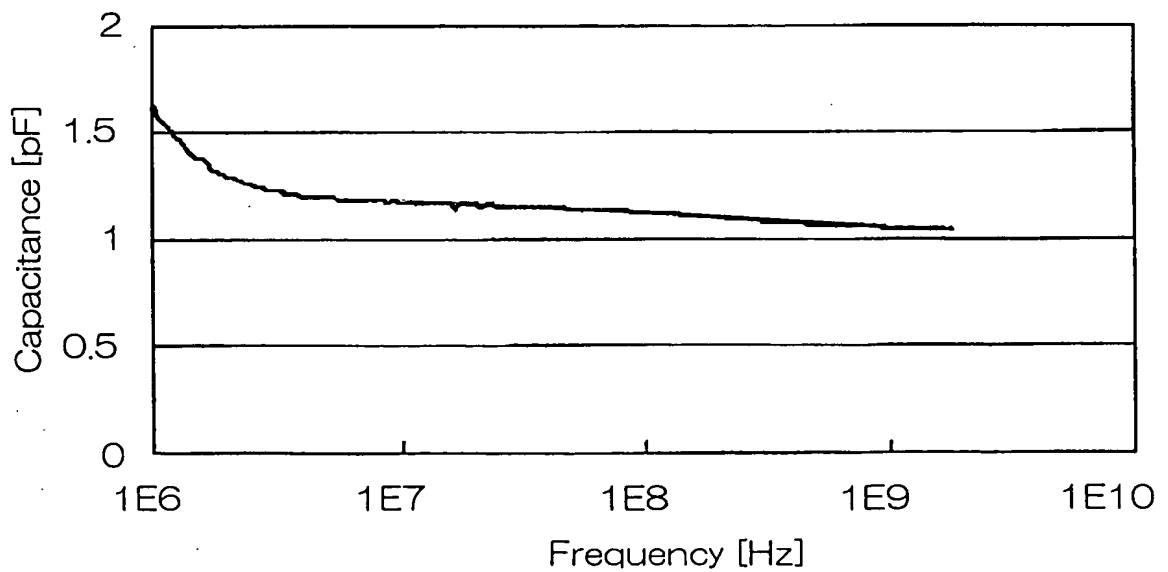




FIG. 17

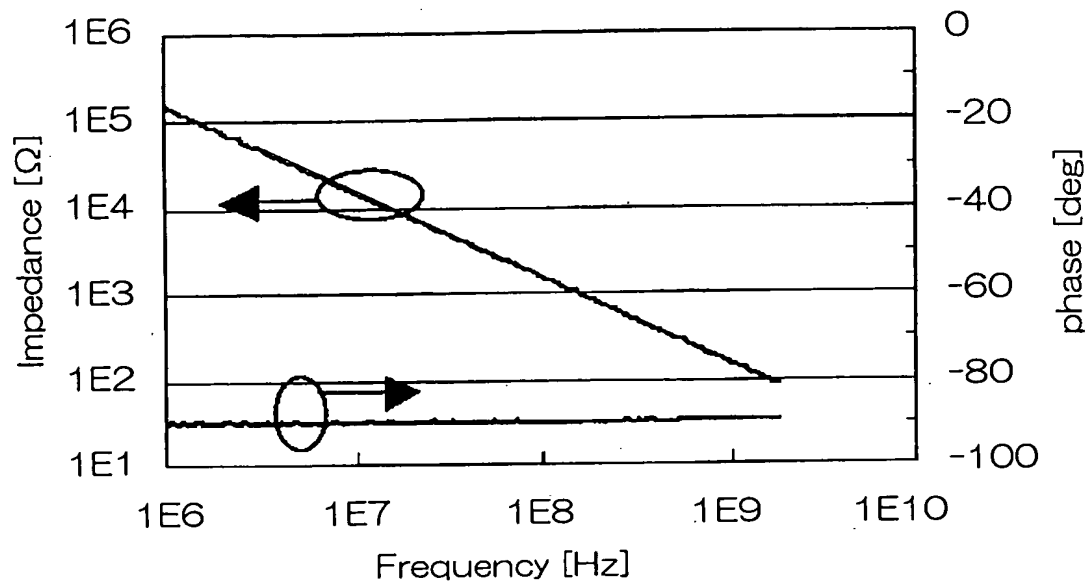


FIG. 18

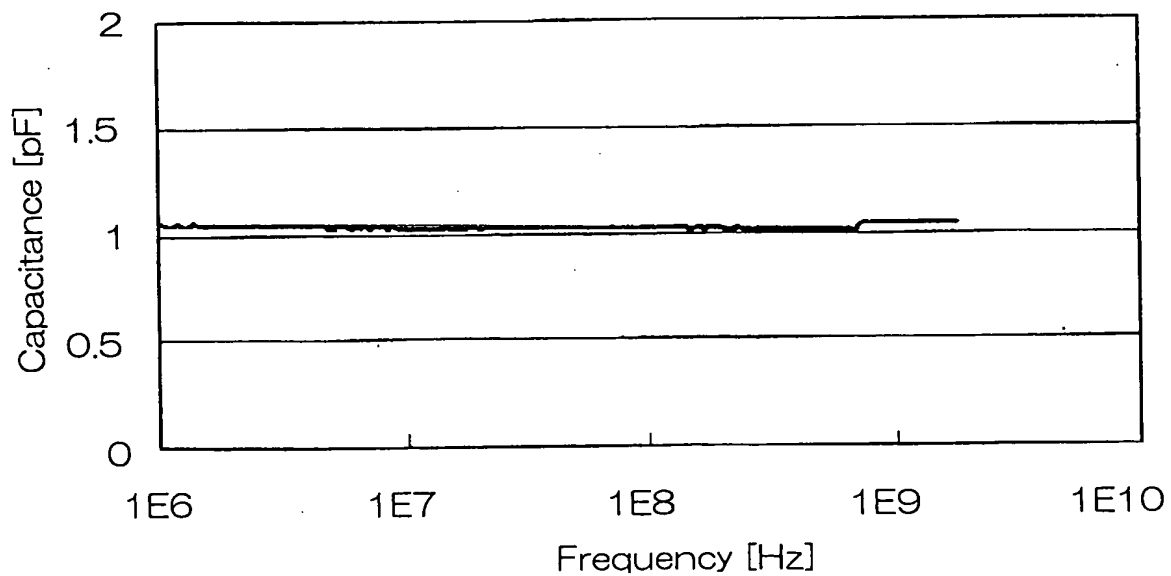


FIG. 19

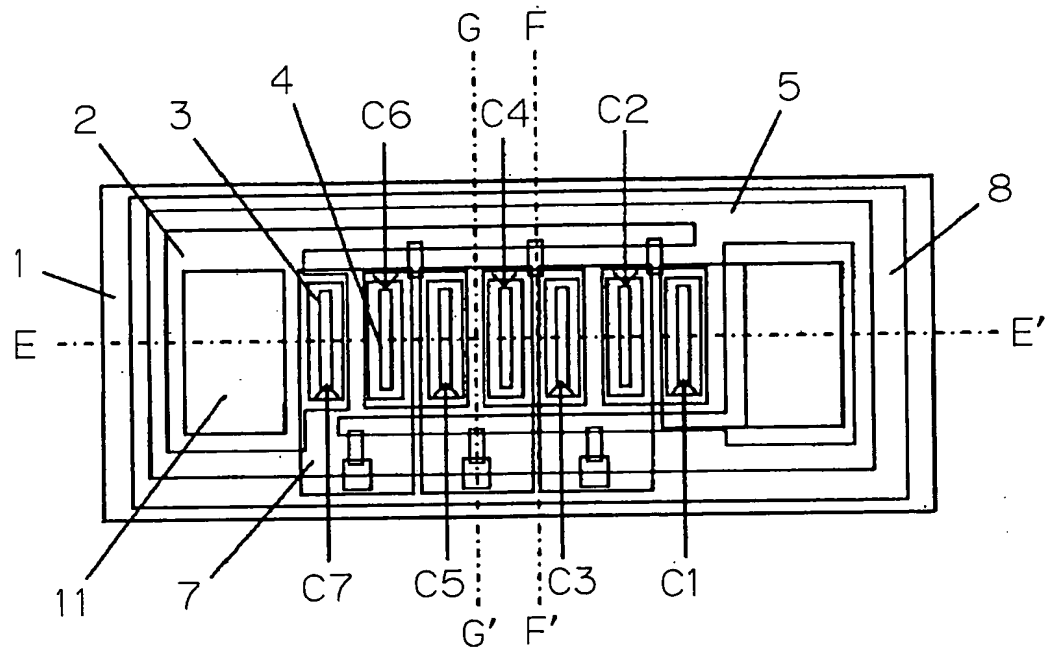


FIG. 20

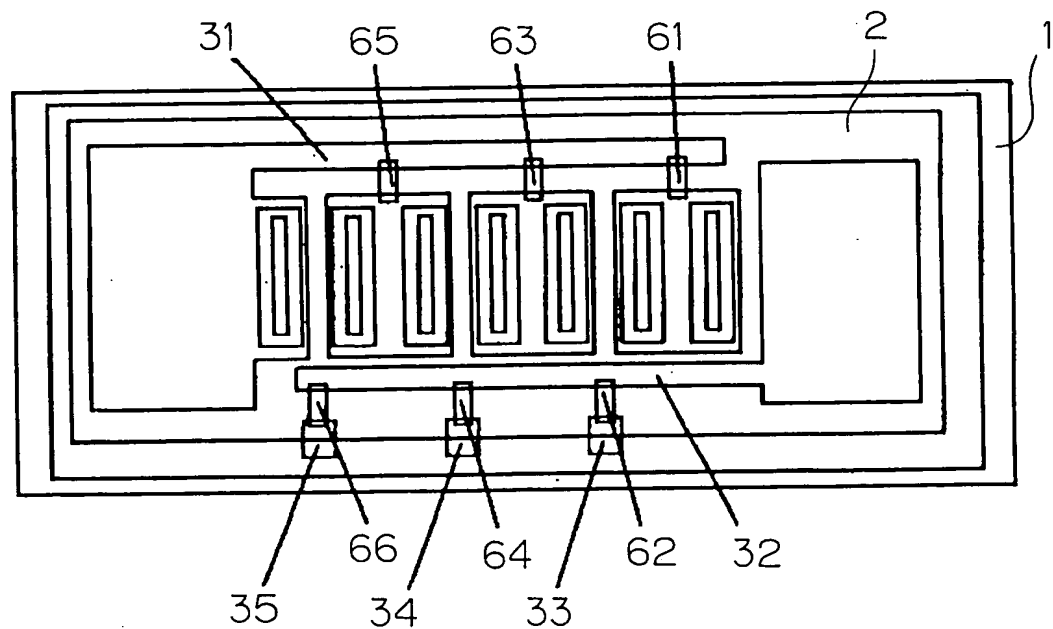


FIG. 21

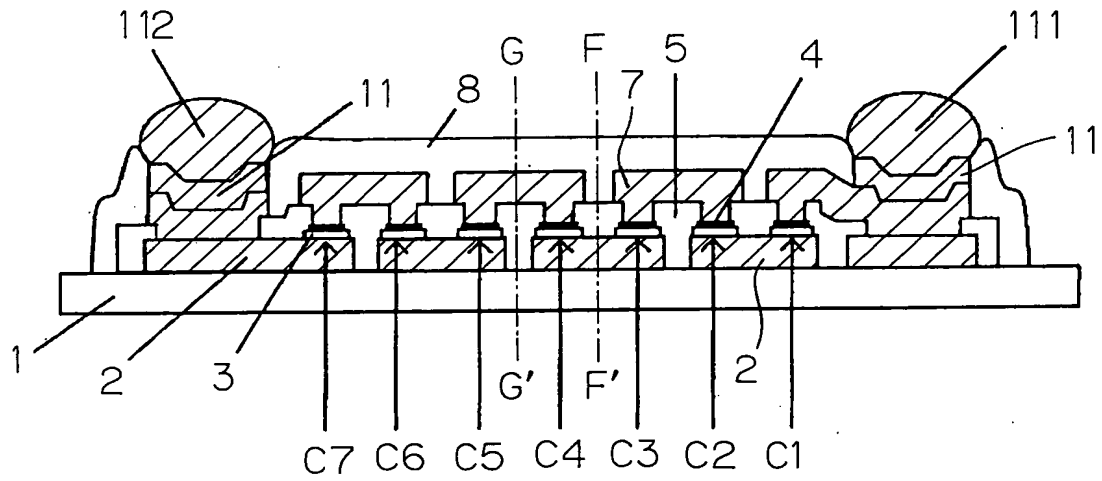


FIG. 22

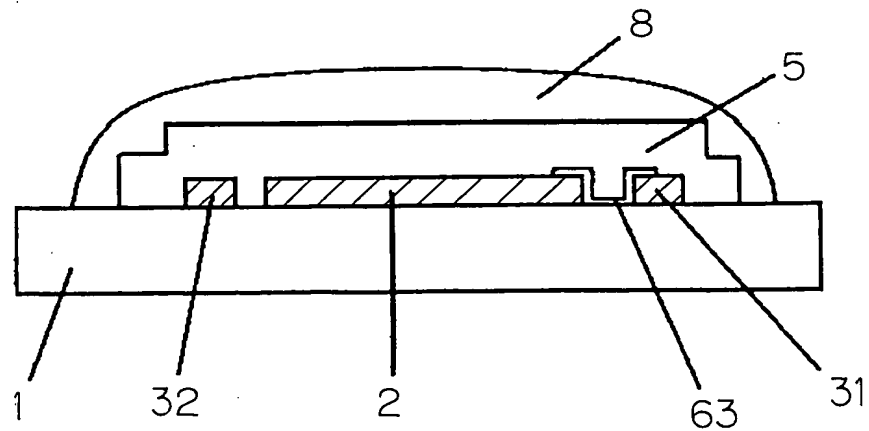


FIG. 23

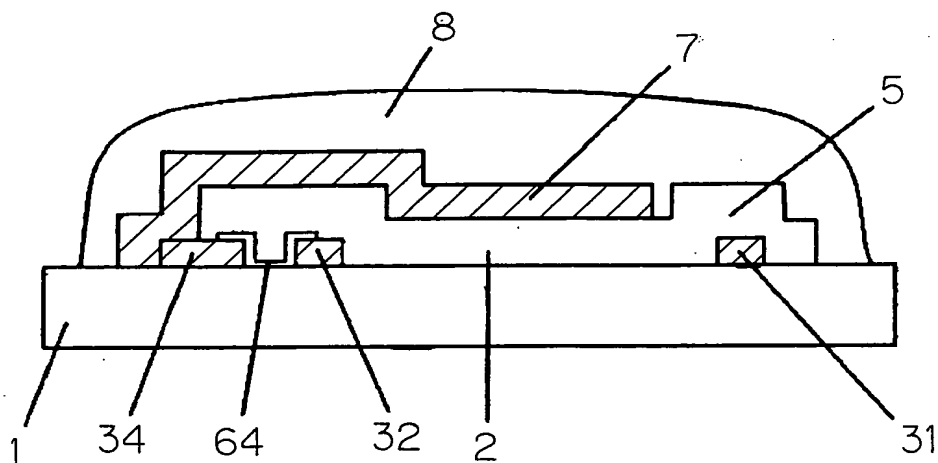


FIG. 24

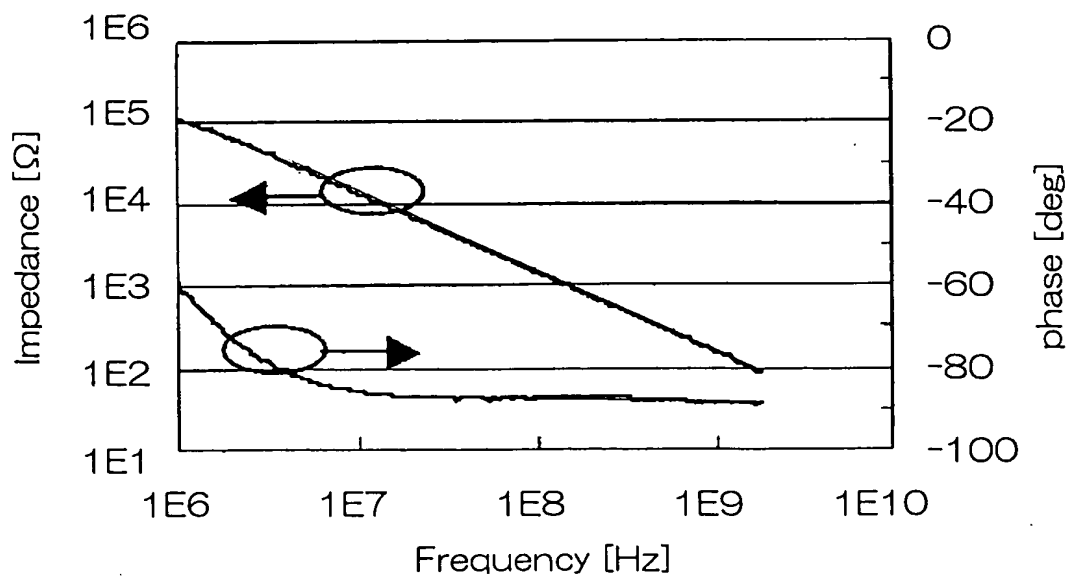


FIG. 25

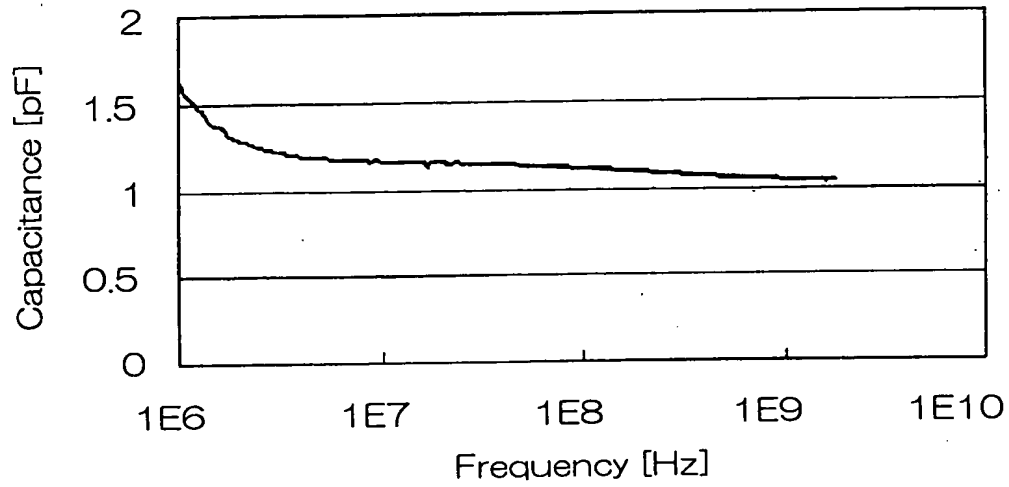


FIG. 26

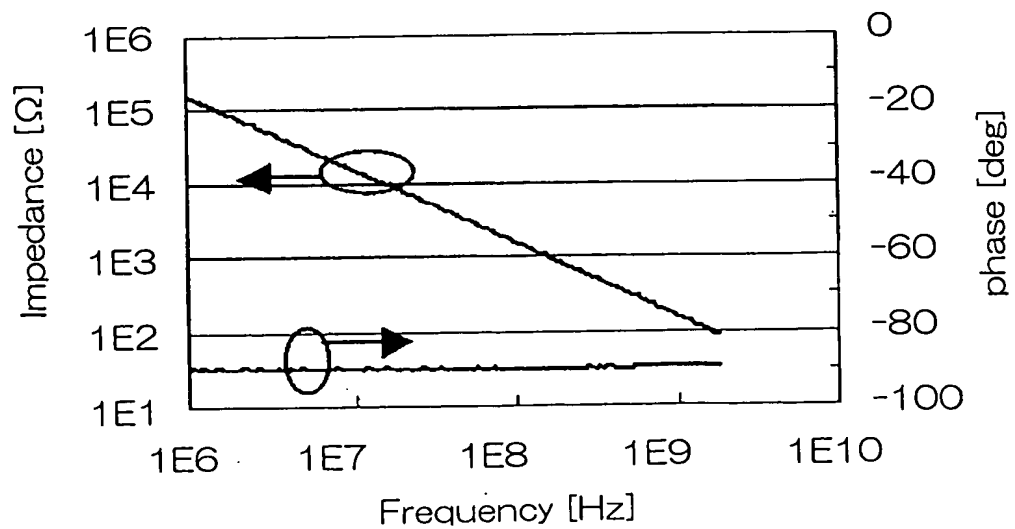


FIG. 27

